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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	75292/13356
First Inventor	Vladislav Vashchenko
Title	HIGH HOLDING VOLTAGE LVTSCR-LIKE STRUCTURE
Express Mail Label No.	EL574678230US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 9] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 7]
5. Oath or Declaration [*Total Pages* 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)
8. Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*)
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [X] Other: Limited Recognition Under 37 CFR Sect. 10.9(b)

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: _____/_____

Prior application information: *Examiner* _____ *Group Art Unit:* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

Name	Jurgen K. Vollrath				
Address	Arter & Hadden, LLP				
	Two Embarcadero Center, 5th Floor				
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Country	USA	*Telephone*	415-617-2100	*Fax*	415-912-3636

Name (Print/Type)	Jurgen K. Vollrath	*Registration No. (Attorney/Agent)*	See attached
Signature	J. Vollrath	*Date*	8/30/01

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	($) 790.00

Complet if Known	
Application Number	
Filing Date	
First Named Inventor	Vladislav Vashchenko
Examiner Name	
Group Art Unit	
Attorney Docket No.	75292/13356

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 01-2520

Deposit Account Name: Arter & Hadden, LLP

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Applicant claims small entity status. See 37 CFR 1.27

2. [X] **Payment Enclosed:**

[X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	8	-20** = 0	X		=0
Independent Claims	4	- 3** = 1	X	40	=40
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 40

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40

SUBMITTED BY

Complete *(if applicable)*

Name (Print/Type)	Jurgen K. Vollrath	*Registration No. (Attorney/Agent)*	See attached	*Telephone*	415-617-2100
Signature	J. Vollrath			*Date*	8/30/01

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REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Vladislav Vashchenko
Title	HIGH HOLDING VOLTAGE LVTSCR-LIKE STRUCTURE
Atty Docket Number	75292/13356

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

8/30/01
Date

J. Vollrath
Signature

Jurgen K. Vollrath
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

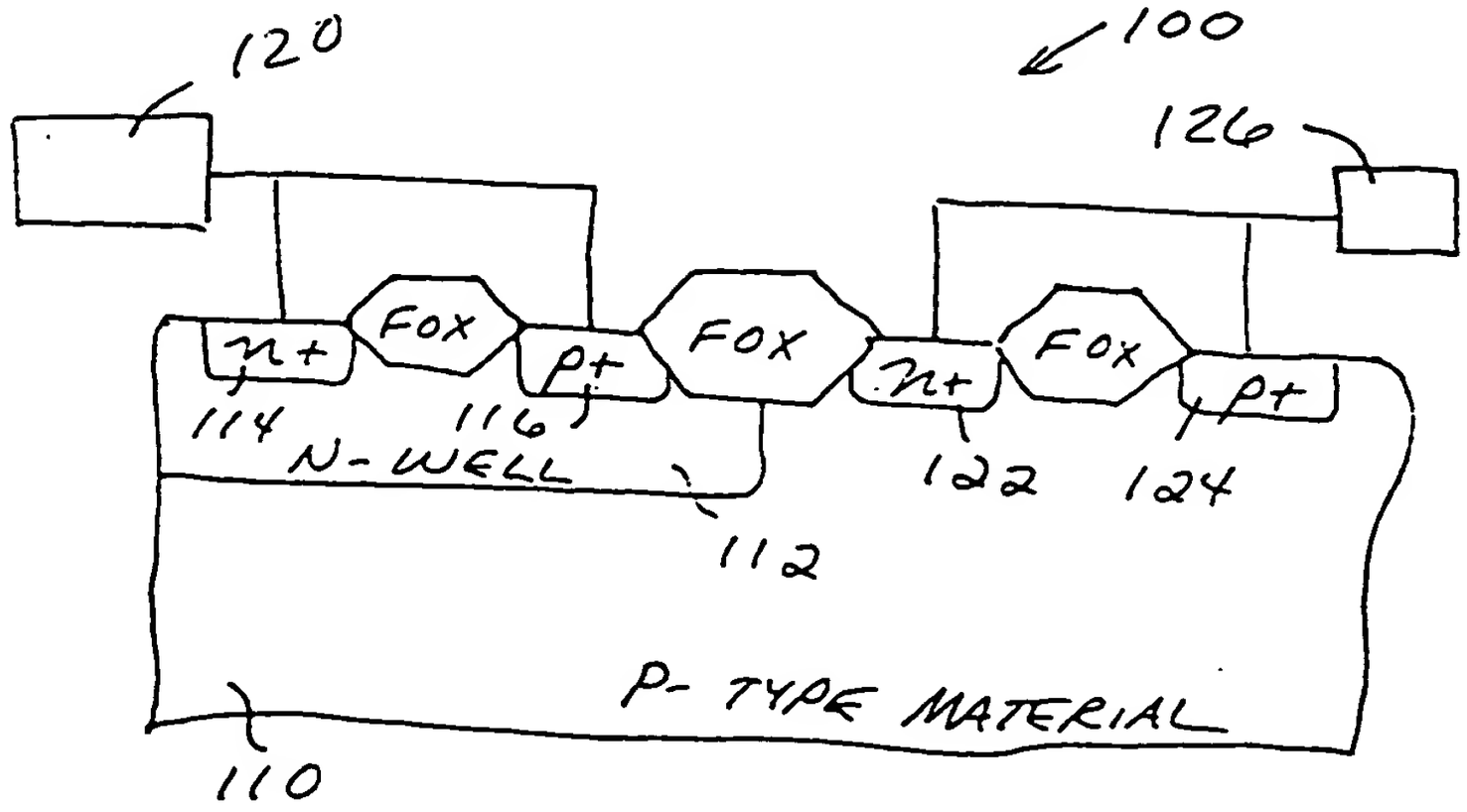


FIG. 1
(PRIOR ART)

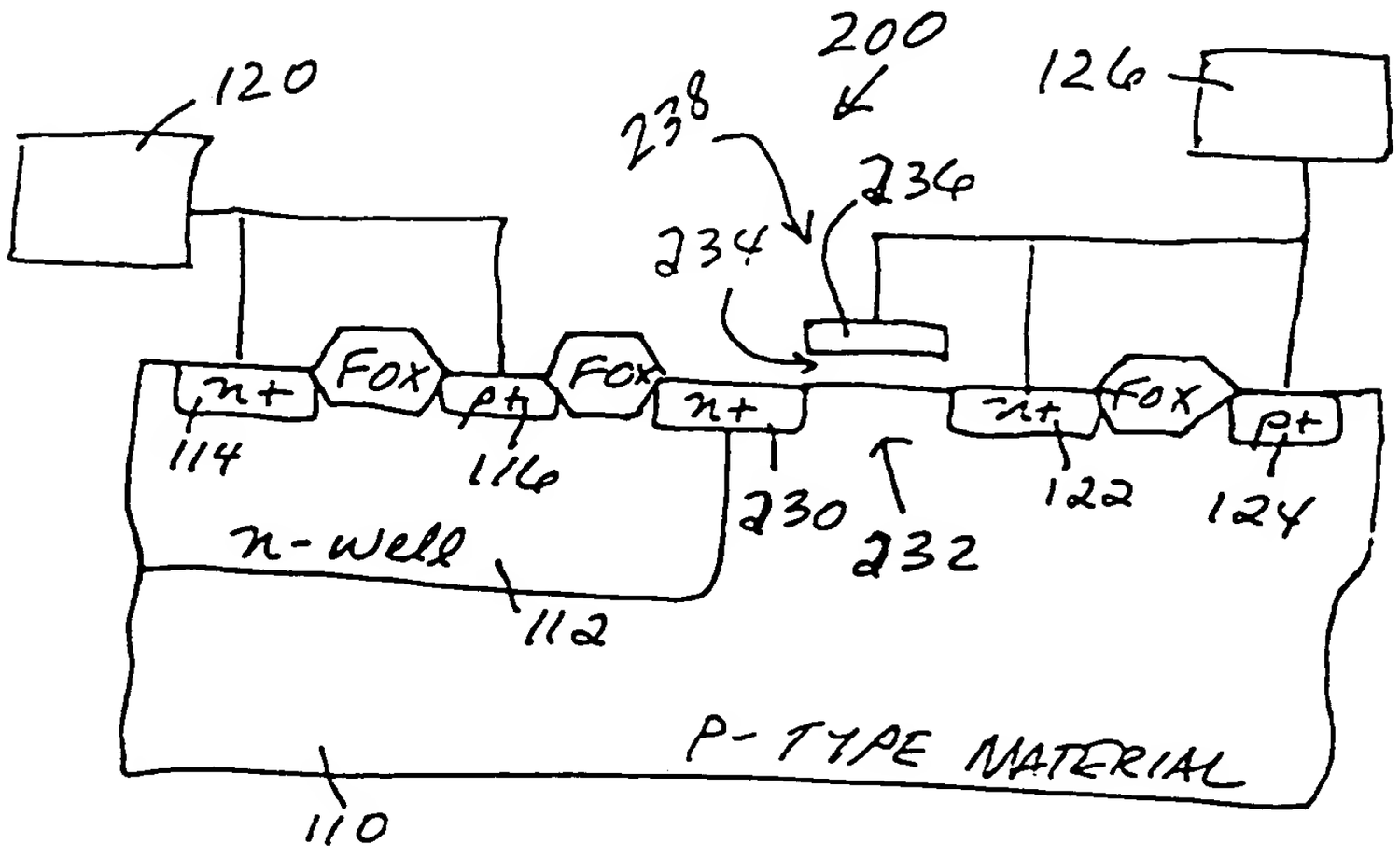


FIG. 2
(PRIOR ART)

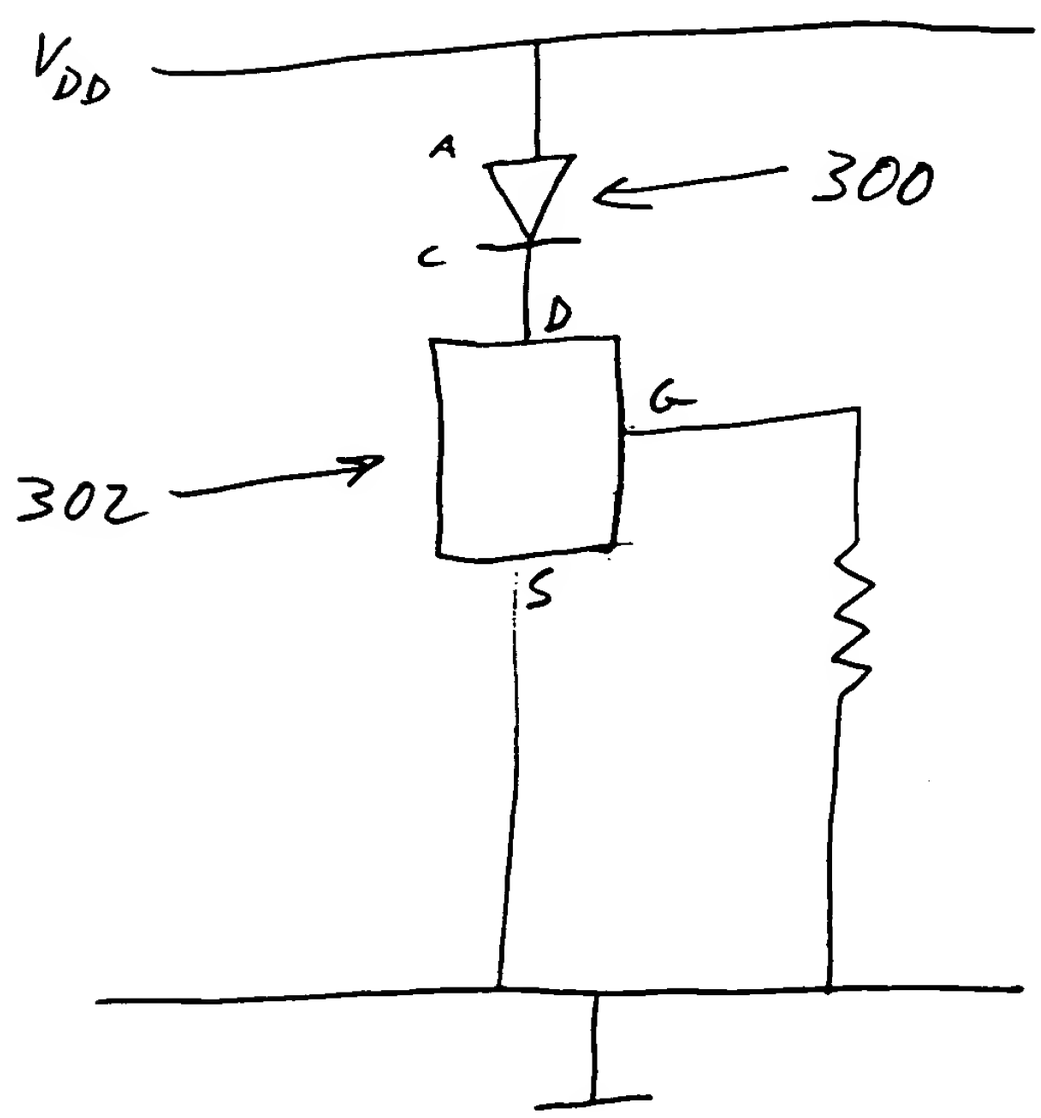


Fig 3

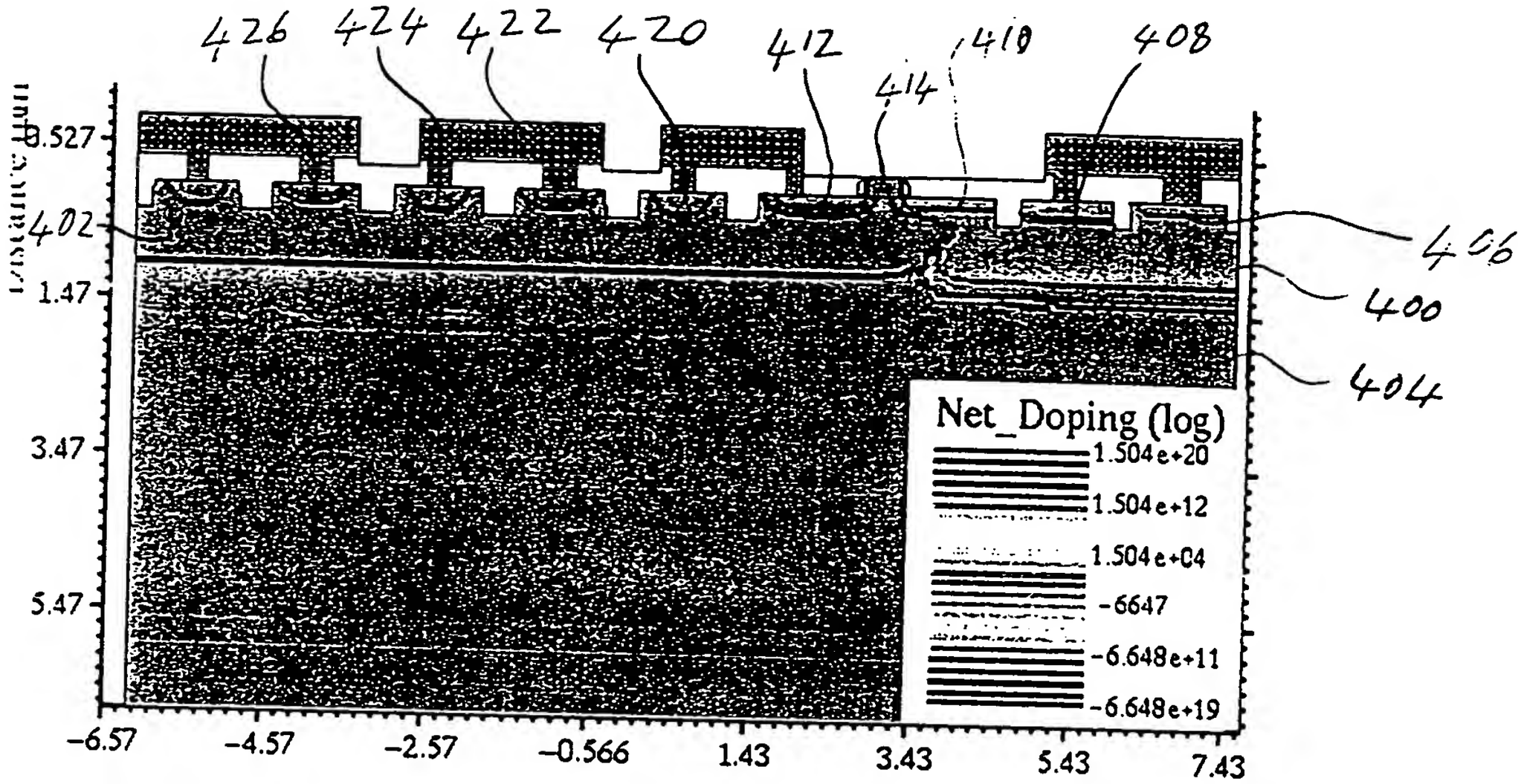


Fig 4

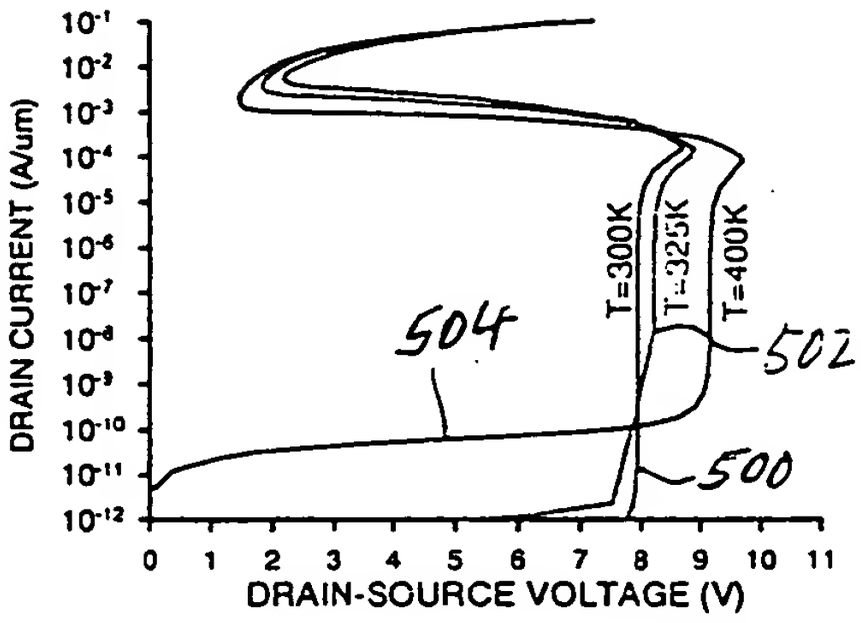


Fig 5

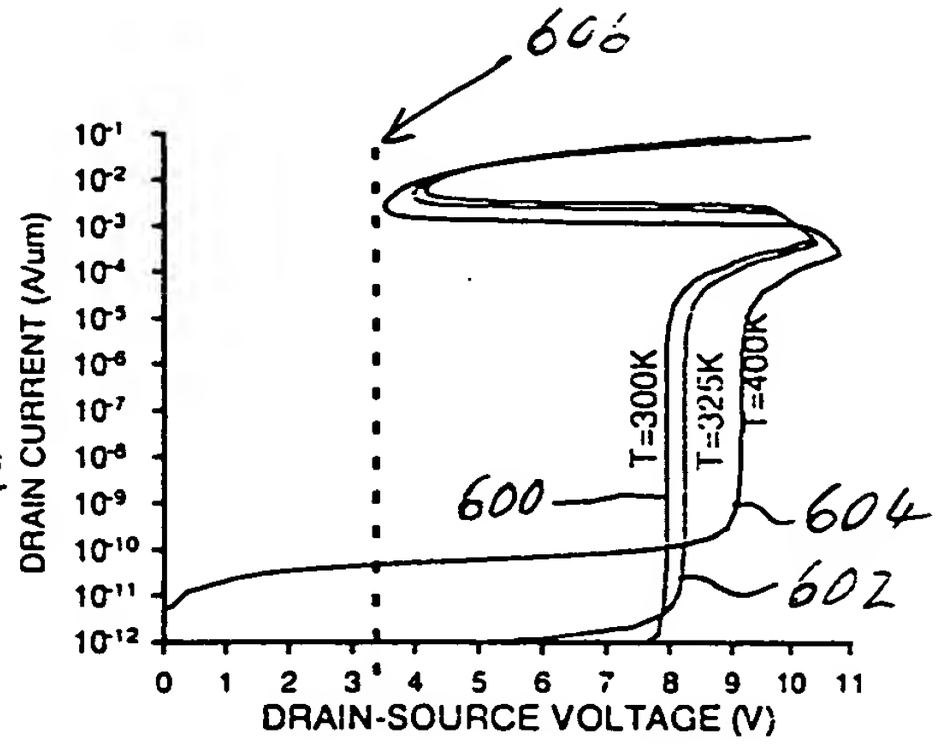


Fig 6

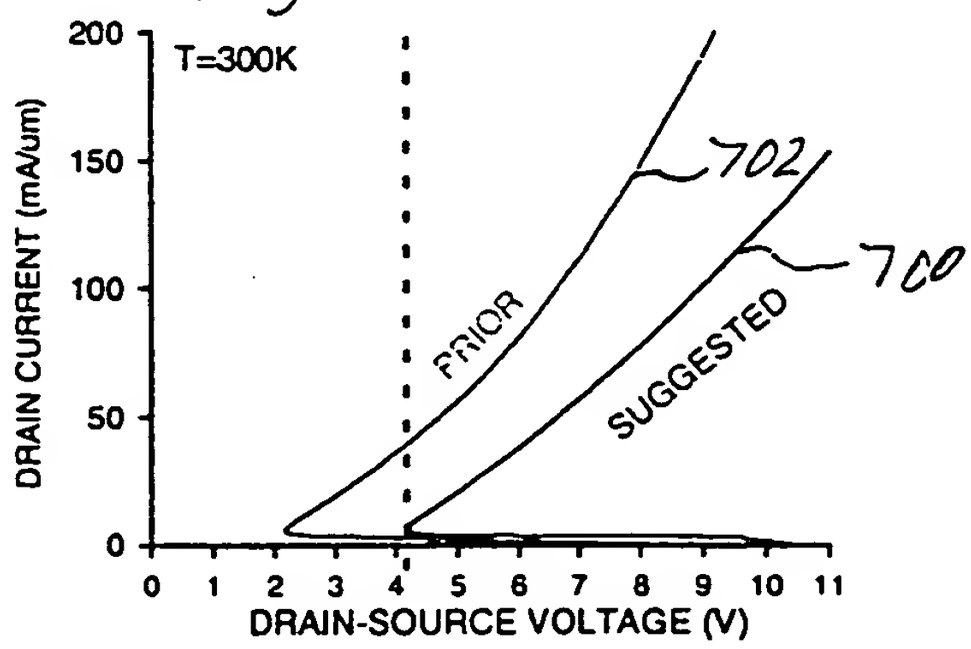


Fig 7

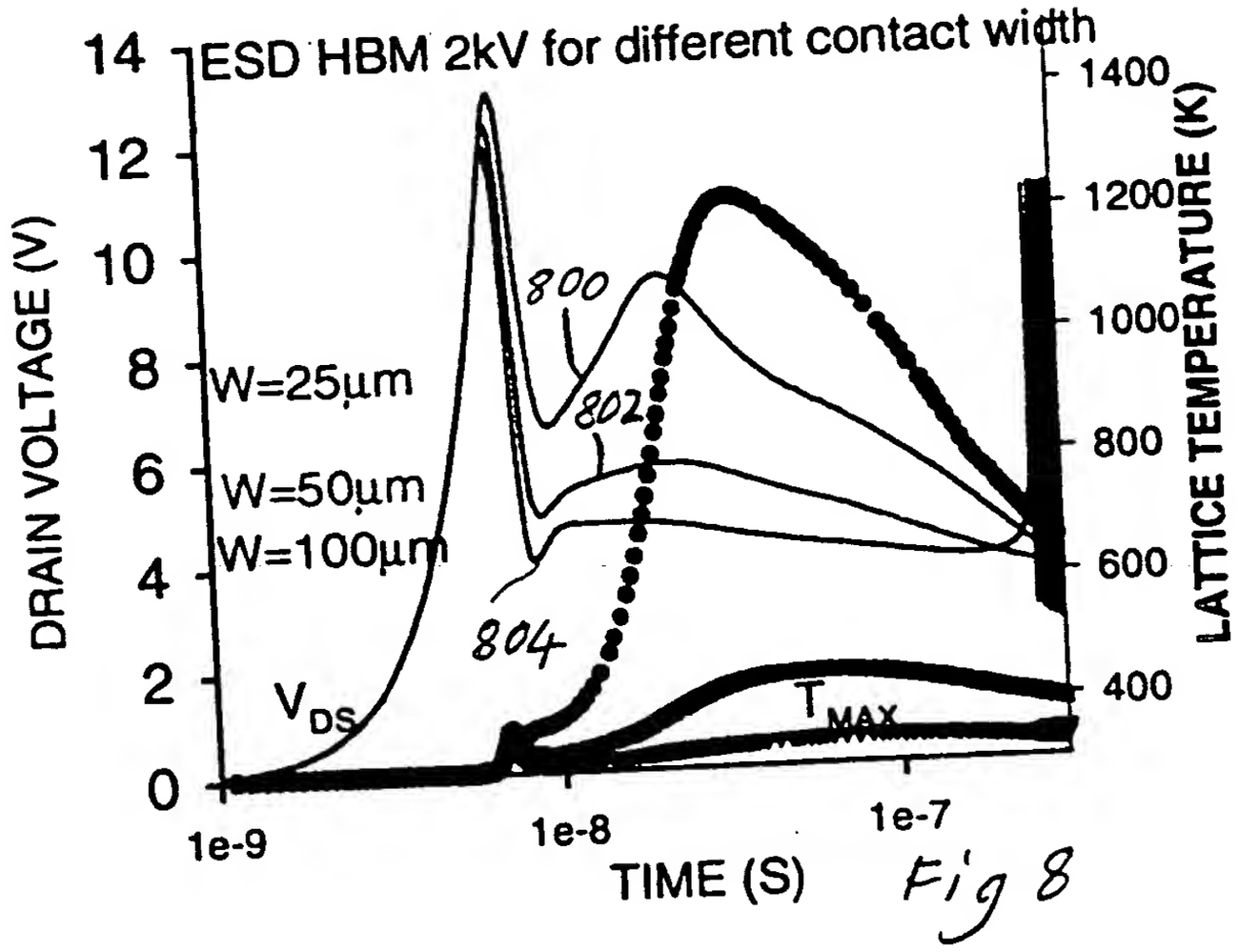


Fig 8

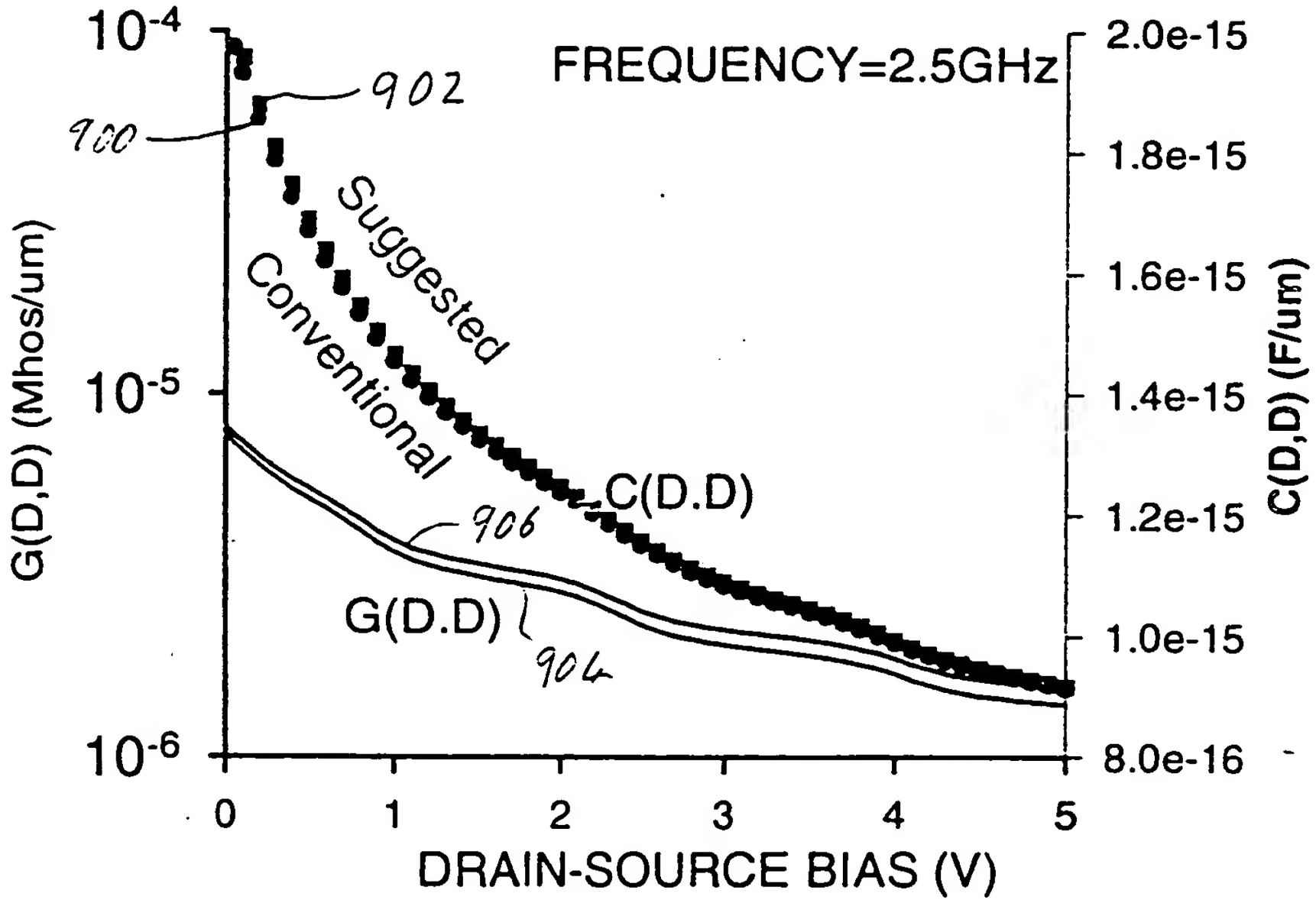
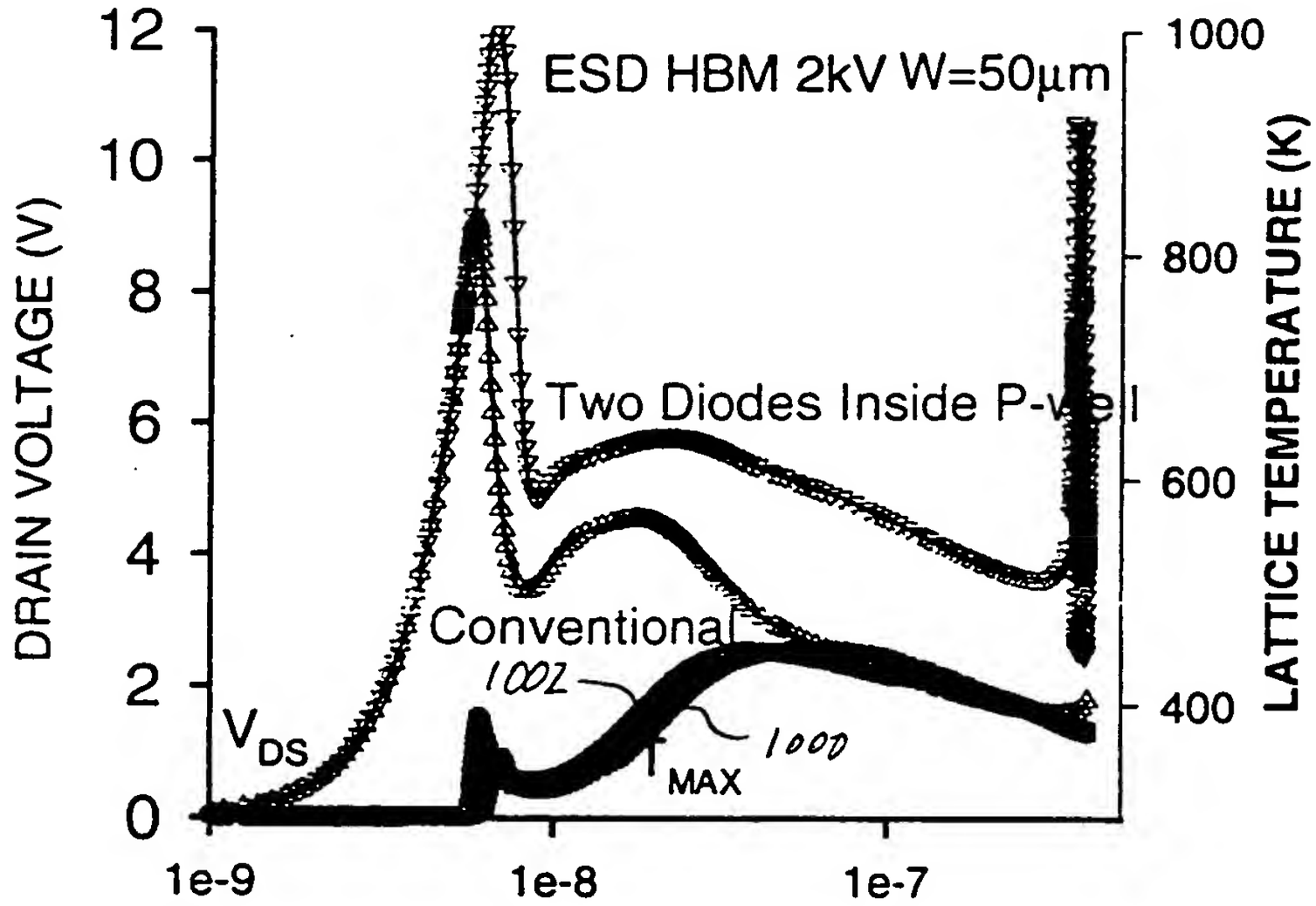


Fig 9

Fig 10



75292/13356

UNITED STATES NON-PROVISIONAL PATENT APPLICATION

for

HIGH HOLDING VOLTAGE LVTSCR-LIKE STRUCTURE

by

Vladislav Vashchenko

Sheets of Drawings: 7

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(415) 912-3636

HIGH HOLDING VOLTAGE LVTSCR-LIKE STRUCTURE

75292/13356

Field of the Invention

The invention relyy7ates to ESD protection devices. More particularly, it relates to LVTSCR-like devices for protecting CMOS and Bi-CMOS integrated circuits against electrostatic discharge and electrical overstress.

Background of the Invention

Analog circuits typically display sensitivity to excessive voltage levels. Transients, such as electrostatic discharges (ESD) can cause the voltage handling capabilities of the analog circuit to be exceeded, resulting in damage to the analog circuit. Clamps have been devised to shunt current to ground during excessive voltage peaks.

One of the difficulties encountered in designing such protection circuitry is that the specifications for these clamps have to fit within a relatively small design window that, on the one hand, must take into account the breakdown voltage of the circuit being protected, and, on the other hand, avoid latch-up under normal operation. Thus, the clamp must be designed so as to be activated below the breakdown voltage of the circuit that is to be protected. At the same time, the latch-up or holding voltage must exceed the normal operating voltage of the protected circuit.

Some protection clamps employ avalanche diodes such as zener diodes to provide the bias voltage for the base of a subsequent power bipolar junction transistor (BJT).

Grounded gate NMOS devices (GGNMOS) have also been used as ESD protection devices. However, GGNMOS devices are not only large, consuming a lot of space on a chip, they also suffer from the disadvantage that they support only limited current densities. The protection capability of an ESD protection device can be defined as the required contact width of the structure required to protect against an ESD pulse amplitude, or, stated another way, as the maximum protected ESD pulse amplitude for a given contact width. Thus, the smaller the contact width for a given ESD pulse amplitude protection, the better. One possible ESD protection solution is to use a silicon-controlled rectifier (SCR).

A silicon-controlled rectifier (SCR) is a device that provides an open circuit between a first node and a second node when the voltage across the first and second nodes is positive and less than a trigger voltage. When the voltage across the first and second nodes rises to be equal to or greater than the trigger voltage, the SCR provides a low-resistance current path between the first and second nodes. Further, once the low-resistance current path has been provided, the SCR maintains the current path as long as the voltage across the first and second nodes is equal to or greater than a holding voltage that is lower than the trigger voltage. As a result of these characteristics, SCRs have been used to provide ESD protection. When used for ESD protection, the first node becomes a to-be-protected node, and the second node is typically connected to ground. The SCR operates within an ESD protection window that has a maximum voltage defined by the destructive breakdown level of the to-be-protected node, and a minimum voltage (also known as a latch-up voltage) defined by any dc bias on the to-be-protected node.

Thus, when the voltage across the to-be-protected node and the second node is less than the trigger voltage, the SCR provides an open circuit between the to-be-protected node and the second node. However, when the to-be-protected node receives a voltage spike that equals or exceeds the trigger voltage, such as when an ungrounded human-body discharge occurs, the SCR provides a low-resistance current path from the to-be-protected node to the

second node. In addition, once the ESD event has passed and the voltage on the to-be-protected node falls below the holding voltage, the SCR again provides an open circuit between the to-be-protected node and the second node.

FIG. 1 shows a cross-sectional view that illustrates a conventional SCR 100. As shown in FIG. 1, SCR 100 has a n-well 112 which is formed in a p-type semiconductor material 110, such as a substrate or a well, and a n+ region 114 and a p+ region 116 which are formed in n-well 112. The n+ and p+ regions 114 and 116 are both connected to a to-be-protected node 120. As further shown in FIG. 1, SCR 100 also has a n+ region 122 and a p+ region 124 formed in semiconductor material 110. The n+ and p+ regions 122 and 124 are both connected to an output node 126.

In operation, when the voltage across nodes 120 and 126 is positive and less than the trigger voltage, the voltage reverse biases the junction between n-well 112 and p-type material 110. The reverse-biased junction, in turn, blocks charge carriers from flowing from node 120 to node 126. However, when the voltage across nodes 120 and 126 is positive and equal to or greater than the trigger voltage, the reverse-biased junction breaks down due to avalanche multiplication.

The breakdown of the junction causes a large number of holes to be injected into material 110, and a large number of electrons to be injected into n-well 112. The increased number of holes increases the potential of material 110 in the region that lies adjacent to n+ region 122, and eventually forward biases the junction between material 110 and n+ region 122.

When the increased potential forward biases the junction, a npn transistor that utilizes n+ region 122 as the emitter, p-type material 110 as the base, and n-well 112 as the collector turns on. When turned on, n+ (emitter) region 122 injects electrons into (base) material 110. Most of the injected electrons diffuse through (base) material 110 and are swept from (base) material 110 into (collector) n-well 112 by the electric field that extends across the reverse-biased junction. The electrons in (collector) n-well 112 are then collected by n+ region 114.

A small number of the electrons injected into (base) material 110 recombine with holes in (base) material 110 and are lost. The holes lost to recombination with the injected electrons are replaced by holes injected into (base) material 110 by the broken-down reverse-biased junction and, as described below, by the collector current of a pnp transistor, thereby providing the base current.

The electrons that are injected and swept into n-well 112 also decrease the potential of n-well 112 in the region that lies adjacent to p+ region 116, and eventually forward bias the junction between p+ region 116 and n-well 112. When the decreased potential forward biases the junction between p+ region 116 and n-well 112, a pnp transistor formed from p+ region 116, n-well 112, and material 110, turns on.

When turned on, p+ emitter 116 injects holes into base 112. Most of the injected holes diffuse through (base) n-well 112 and are swept from (base) n-well 112 into (collector) material 110 by the electric field that extends across the reverse-biased junction. The holes in (collector) material 110 are then collected by p+ region 124.

A small number of the holes injected into (base) n-well 112 recombine with electrons in (base) n-well 112 and are lost. The electrons lost to recombination with the injected holes are replaced by electrons flowing into n-well 112 as a result of the broken-down reverse-biased junction, and n-well 112 being the collector of the npn transistor. Thus, a small part of the npn collector current forms the base current of the pnp transistor.

Similarly, as noted above, the holes swept into (collector) material 110 also provide the base current holes necessary to compensate for the holes lost to recombination with the diffusing electrons injected by n+ (emitter) region 122. Thus, a small part of the pnp collector current forms the base current of the npn transistor.

Thus, n+ region 122 injects electrons that provide both the electrons for the collector current of the npn transistor as well as the electrons for the base current of the pnp transistor. At the same time, p+ region 116 injects holes that provide both the holes for the collector current of the pnp transistor as well as the holes for the base current of the npn transistor.

One of the advantages of SCR 100 over other ESD protection devices, such as a grounded-gate MOS transistor, is the double injection provided by n+ region 122 and p+ region 116 of SCR 100. With double injection, SCR 100 provides current densities (after snapback) that are about ten times greater than the densities provided by a grounded-gate MOS device.

One of the disadvantages of SCR 100, however, is that a very large positive voltage, e.g., 50 volts, must be dropped across nodes 120 and 126 before the junction between p-type material 110 and n-well 112 breaks down. As a result, SCR 100 can not be used to protect devices, such as MOS transistors, that can be permanently damaged by much lower voltages, e.g., 15 volts.

One solution proposed in the past, was to use low voltage silicon controlled rectifiers (LVTSCRs) which are not only smaller but allow the reaching of current densities, after snap back, that are some ten times higher than the current densities of traditionally used grounded gate NMOS devices (GGNMOS), thus increasing the ESD protection capability for CMOS circuits.

An LVTSCR incorporates a NMOS transistor into SCR 100. FIG. 2 shows a cross-sectional diagram that illustrates a conventional LVTSCR 200. LVTSCR 200 and SCR 100 are similar and, as a result, utilize the same reference numerals to designate the structures that are common to both devices.

As shown in FIG. 2, LVTSCR 200 differs from SCR 100 in that LVTSCR 200 has a n+ (drain) region 230 that is formed in both material 110 and n-well 112, and a channel region 232 that is defined between n+ (source) region 122 and n+ (drain) region 230. In addition, LVTSCR 200 includes a gate oxide layer 234 that is formed on material 110 over channel region 232, and a gate 236 that is formed on gate oxide layer 234. N+ (source and drain) regions 122 and 230, gate oxide layer 234, and gate 236 define a NMOS transistor 238 which is typically formed to be identical to the to-be-protected MOS transistors in the circuit.

In operation, when the voltage on the drain of a conventional NMOS transistor spikes up, the drain-to-substrate junction of the NMOS transistor breaks down, for example, at 7 volts, while the gate oxide layer that isolates the gate from the drain destructively breaks down at, for example, 10-15 volts.

Since NMOS transistor 238 is formed to be identical to the to-be-protected MOS transistors, the junction between n+ region 230 and material 110 breaks down at the same time that the to-be-protected MOS transistors experience junction break down as a result of an ESD pulse. Once the reverse-biased junction between region 230 and material 110 breaks down, the break down triggers LVTSCR 200 to operate the same as SCR 100.

Since junction break down occurs before the MOS transistors experience destructive gate oxide break down, LVTSCR 200 turns on before destructive gate oxide breakdown occurs, thereby protecting the MOS transistors. Thus, the junction breakdown voltage, which is less than the voltage level that causes destructive gate

oxide break down, functions as the trigger voltage. In addition, other techniques, such as reducing the width of channel region 232, can be used to lower the trigger voltage so that the region 230 to material 110 junction breaks down before the to-be-protected MOS transistors experience junction breakdown.

Thus, LVTSCR 200 provides a SCR with a significantly lower turn-on voltage that allows MOS transistors to be protected from ESD events with an SCR. However, one disadvantage of LVTSCR 200, and, for that matter, any SCR is that it suffers from a holding voltage that is often less than the minimum (or latch-up) voltage of the ESD protection window. The low holding voltage of the LVTSCR which lies in the range of less than two volts, is due to the double junction injection of its conductivity modulation mechanism. While the p+ emitter allows one to define how many holes are injected, the injection of the holes leads to greater space charge neutralization and thus a lower holding voltage. As a result, standard LVTSCRs are unattractive candidates for providing ESD protection to power supply pins.

As mentioned above, the major requirement when designing ESD protection circuits, is that the circuit operate within a so-called "ESD protection window" that is usually limited by both the maximum voltage in the protected line (which is related to the breakdown of the protected circuits) and the latch-up voltage when the DC bias is presented in the protected line.

In the LVTSCR, when the minimum (or latch-up) voltage of the ESD protection window is equal to a dc bias, such as the power supply voltage, LVTSCR 200 cannot turn off (thus latching up) after the ESD event has passed. Thus, power must be cycled after the ESD event, to switch off the LVTSCR.

For example, assume that node 120 is a power supply pin at 3.3 volts, node 126 is a ground pin, the junction breakdown voltages of the to-be-protected MOS transistors are 7.0 volts, and the holding voltage is 1.8 volts. In this example, LVTSCR 200 is turned off under normal operating conditions when the voltage on node 120 is 3.3 volts. When the voltage on node 120 spikes up to a value equal to or greater than the trigger voltage (7 volts in this example), LVTSCR 200 turns on, thereby protecting the MOS devices that receive power from node 120. However, once the ESD event has passed, since the normal operating voltage on node 120 is 3.3 volts, and it takes only 1.8 volts on node 120 to keep LVTSCR 200 in this example turned on, LVTSCR 200 remains turned on (latched up) after the ESD event has passed.

Thus, in spite of higher current availability from an LVTSCR after snap back, conventional CMOS integrated circuits are usually protected by grounded gate NMOS snap back structures (GGNMOS) due to the latch-up limitations of LVTSCRs.

What is needed is a device that fills the void between low current GGNMOS devices and low holding voltage, high current SCR and LVTSCR devices.

One proposed solution to increasing the holding voltage of a LVTSCR has been to provide a circuit in conjunction with the LVTSCR which increases the holding voltage by introducing a voltage drop in the form of one or more diodes. This is illustrated in Figure 3 in which a diode 300 is connected in series with the LVTSCR 302 between V_{dd} and ground. The problem with such an isolated diode or diodes string is that it increases the parasitic capacitance and consumes more space. Furthermore, it is not suitable for all CMOS processes and therefore does not lend itself steadily to implementation using existing process technology.

Summary of the Invention

The present invention provides an LVTSCR-like structure having an increased holding voltage.

Further, according to the invention, there is provided a LVTSCR-like ESD protection structure having one or more diodes formed in a p-well of the structure.

Further, according to the invention, there is provided a method of increasing the holding voltage of a LVTSCR structure, comprising forming at least one p-n junction inside a p-well of the structure.

Still further, according to the invention, there is provided a method of increasing the holding voltage of a LVTSCR-like structure, comprising providing an alternative current path through a p-well of the structure, other than the pure p-material of the p-well. The current path forming a lower resistance current path than the p-well. The low resistance current path may take the form of p-n junctions formed in the p-well. Thus, diodes are formed in the p-well which provide a low resistance current path once the voltage across the one or more diodes are exceeded.

Brief Description Of The Drawings

Figure 1 is a cross-sectional view of a conventional SCR;

Figure 2 is a cross-sectional view of a conventional LVTSCR;

Figure 3 is a schematic circuit diagram of a LVTSCR protection circuit connected in series with a diode;

Figure 4 is a cross-sectional view of one embodiment of a LVTSCR-like structure of the invention;

Figure 5 are I-V curves at different temperatures for a conventional LVTSCR;

Figure 6 are I-V curves at different temperatures for one embodiment of a device of the invention;

Figure 7 are comparative I-V curves for a conventional LVTSCR and one embodiment of the invention, at high currents;

Figure 8 shows drain voltage-time curves and lattice temperature-time curves at different widths for one embodiment of the invention;

Figure 9 are conduction and capacitance curves plotted against bias voltage for a conventional LVTSCR and one embodiment of a device of the invention.

Figure 10 shows temperature-time and drain voltage-time curves for a conventional device and a device of the invention.

Detailed Description of the Invention

One embodiment of a LVTSCR-like structure of the invention is illustrated in Figure 4 in which a n-well 400 and a p-well 402 are formed in a substrate 404. As in the case of a conventional LVTSCR, a n+ drain region 406 and p+ emitter/drain 408 are formed in the n-well 400. A floating drain 410 is also formed in the n-well 400, and extends into the p-well 402. A n+ source 412 is formed in the p-well 402, and a gate 414 is defined over a channel region between the floating drain 410 and the n+ source 412. Furthermore, the embodiment of the invention illustrated in Figure 4 includes two diodes comprising a first p+ region 420, a first n+ region 422, a second p+ region 424, and a second n+ region 426 formed in the p-well 402. The first p+ and n+ regions 420, 422 define the anode and cathode respectively of a diode formed in the p-well, by defining a p-n junction in the p-well.

The second p+ and n+ regions 424, 426 define the anode and cathode respectively of a second diode formed in the p-well 402.

A low currents before the threshold voltage of the diodes is exceeded, current flows substantially through the p-well since the diodes are essentially short circuited by the p-well resistance. Therefore, the breakdown and triggering voltages are not adversely effected by the addition of the diodes, as is illustrated in Figures 5 and 6. Figure 5 shows drain current against drain-source voltage for a conventional LVTSCR at 300K (curve 500), at 325K (curve 502), and at 400K (curve 504). Figure 6 shows drain current against drain-source voltage for one embodiment of the invention for temperatures of 300K, 325K, and 400K as indicated by curves 600, 602, 604, respectively. As can be seen by the vertical line 606, the holding voltage for the device of the invention is substantially higher than that for the conventional LVTSCR, whereas the breakdown and triggering voltages are substantially the same as for the conventional device.

At high currents after triggering, the internal diode current path is used which defines a correspondingly higher holding voltage as determined by the SCR structure and the two diodes, thereby defining a holding voltage of approximately 1.5V plus two times 1V. This is evident in Figure 6, which shows a higher holding voltage, as defined by the vertical line 606. This is also illustrated in Figure 7 which shows the drain current against drain-source voltage for a device of the invention (curve 700) compared to that of a conventional LVTSCR (Curve 702).

The present invention displays a number of advantages over the prior art. It provides for a simple interconnect layout and a compact design by providing a straightforward serial arrangement. Simulation results have also shown that compared to prior art high holding voltage SCR designs, the present invention displays little sensitivity to process variations, doping levels, and dimension variations. Figure 8 shows voltage curves 800, 802, and 804 for widths w=25m, 50m, and 100m, respectively. Furthermore, since the diodes are formed inside the grounded p-well 402, the structure does not increase the capacitance over that of a conventional LVTSCR. This is illustrated by the curves in Figure 9 showing the capacitance variation with drain-source bias for a conventional device (curve 900) compared to that of a device of the invention (curve 902). Figure 9 also shows that the conductance curves for a device of the invention (curve 904) remains essentially the same as that for a conventional LVTSCR (curve 906). Furthermore, the holding voltage displays a low temperature curve. Referring to Figure 10, the lattice temperature variation for a device of the invention (curve 1000) is substantially the same as that for a conventional device (curve 1002). Also, the holding voltage is shown to be higher for the device of the invention.

According to TCAD simulations, for a 2kV HBM pulse, ESD protection with a holding voltage of more than 3.5V can be achieved with an initial substrate temperature range of less than 400K, even at a 25 μm contact with. This was also shown to have a parasitic compacitance of below 14 fF.

It will be appreciated that the p-n structures formed in the p-well of the structure may vary in number and shape, and that the invention can be implemented in a number of ways to achieve an alternative current path at high currents, other than a current path through the p-well, wherein the alternative current path defines a voltage drop which increases the holding voltage of the structure.

What is claimed is:

1. A LVTSCR-like structure having one or more diodes formed in a p-well of the structure.

2. A method of increasing the holding voltage of a LVTSCR structure, comprising forming at least one p-n junction inside a p-well of the structure.

3. A method of increasing the holding voltage of a LVTSCR-like structure, comprising providing an alternative current path through a p-well of the structure, other than purely the p-material of the p-well.

4. A method of claim 3, wherein the alternative current path defines a lower resistance current path than the p-well.

5. A method of claim 4, wherein the lower resistance current path takes the form of at least one p-n junction formed in the p-well.

6. A method of claim 4, wherein at least one diode is formed in the p-well which provides a low resistance current path once the voltage across the at least one diode is exceeded.

7. A method of increasing the holding voltage of a LVTSCR-like structure, comprising providing an alternative current path through a p-well of the structure.

8. A method of claim 7, wherein the alternative current path becomes the main current path when the current through the LVTSCR exceeds the saturation current through the resistor formed by the p-well and the p+ regions of the diodes.

Abstract

In an ESD protection device making use of a LVTSCR structure, the holding voltage is increased by forming diodes in the p-well of the LVTSCR structure. This provides an alternative current path at high currents and provides a defined voltage drop thereby increasing the holding voltage.

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney D cket Number	75292/13356
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COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH HOLDING VOLTAGE LVTSCR-LIKE STRUCTURE

(Title of the Invention)

the specification of which

[X] is attached hereto

OR

[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

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Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	Certified Copy Attached? NO
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First Named Inventor	Vladislav Vashchenko,
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Attorney Docket Number	75292/13356

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